PCI Express

Course 703 – 32 Hours

Overview

The course provides a detailed and comprehensive understanding of the PCI Express technology.
The course is fully up-to-date and supports the latest version of the international specification (2.0). It covers all aspects of the specification from a hardware design perspective and also discusses the software requirements of PCI Express implementations.
This course provides example implementations, and practical guidance that will give a running start on your design.

Course Objectives

The participants will be able to specify performance, define architecture and design hardware platforms and configure the configuration space.

Who Should Attend

This in-depth course is hardware and software oriented. It describes all options and performance, and as a result it is useful for System Architecture as well.

Prerequisites

Attendees should be either experienced hardware or software engineers.

Course Contents

Legacy PCI – Fundamentals (Plug & Play)

- Performance
- Basic architecture
- Memory, I/O, and Configuration space
- Configuration process
- Data transfer
- PCI to PCI Transparent Bridge concept
- Posted & Non-Posted R/W

Introduction to PCI Express

- Why new I/O architecture
- Link and Lane definition
- Root Complex, Switch & Endpoint definition
- Layers overview (Transaction, Data & Physical)
- Card specification (Electrical and Mechanical)
- Advanced Switching (advanced peer to peer communication)

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Mechanical Specification
- Connector types
- Add In Card form factor

Physical Layer
- Electrical Sub Block
- Card Specification
- Design guidelines
- Lanes
- Link State machine
- Link Training process
- Configuration space – Link Capability

Data Link Layer Basics
- Packet Types
- Packet Format
- Data Link Layer Packet (DLLP)
- Timeout
- Retry

Transaction Layer
- Layering Overview
- Transaction Types (Memory, I/O, Configuration, Messages)
- TLP Header Format
- Request Rules
- Completion Rules
- Maximum Packet Size

System Architecture
- ECRC
- Message Type
- Error Signaling
- Flow Control
- Quality of Service (QoS)
- Interrupt Mechanism (INYx & MSI)
- Intel 915G Chipset

Power
- Reset, Clocks, Cut-Through
- Power Management (PM)
- Slot Capability
- Hot Plug – basics
- Hot Plug/ Removal implementation

Configuration Space
- Type 0 Configuration Space
- PCIe Capability Structure (inside legacy configuration space)

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  - PCI Express Capabilities
  - Device Capabilities
  - Link Capabilities
  - Slot Capabilities
  - Root Complex
- Extended capabilities
  - Advanced Error Reporting
  - Virtual Channel

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