USB Architecture

Course 704 – 24 Hours

Overview
The purpose of this course is to provide the student with the theoretical knowledge required for defining and implementing systems based on USB versions 2 & 3.
The course begins with basic concepts and then fully describes in detail USB Architecture (USB2.0 & USB 3.0). The material is fully up-to-date and supports the latest version of the international specification .
The course also partially covers OTG, UTMI, LPM, EHCI and HSIC.
During the course there are many examples which cover all aspects of USB specification.

Course Objectives
By the end of this course, the student will:
Be able to define the required performance and define USB Descriptors
Be able to design and debug USB devices (HW & SW)

Who Should Attend
This course is designed for Project Managers, Software and Hardware Engineers who design and implement USB 2 & 3.

Prerequisites
Attendees should be either experienced hardware or software engineers.

Course Contents

Background & Fundamentals
- USB Motivation
- Bus Topology
- Endpoints
- USB 2.0 Data Flow (Bulk, Isochronous, Interrupt, Control)
- USB 3.0 Basic Concept (Mechanical, Power Management, Packet Routing)
- Super Speed Layers

USB 3.0 Architecture
- Physical Layer
- Protocol Layer
- Link Layer

Power Management
- U0

sales@mabel-tech.com
info@mabel-tech.com
52 Bar Yehuda St. - Nesher
Phone: +972-4-8571119
Fax: +972-4-8570307
דרך בר יהודה 52, נשר
טלפון: 04-8571119
פקס: 04-8570307

- U1
- U2
- U3
- System Exit Latency
- Self & Bus Power Device

Descriptors
- Device States
- Device Class
- Descriptor Tree
- Device Descriptor
- Control Descriptor
- Interface Descriptor
- Endpoint Descriptor
- Endpoint Companion Descriptor
- BOS

Control Transfer
- USB 2.0 Control Transfer
- USB 3.0 Control Transfer
- Setup – Standard Request Code

USB Hub
- Hub Architecture
- Hub Routing & Signaling
- Hub Descriptors
- Port Status

Examples
- Configuration Device
- HID Class
- Mass Storage Class
- USB 3.0 Tracer Plot

Supplement Specifications
- OTG
- HSIC
- UTMI
- EHCI
- USB3.1 Main Features

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